In the Claims

Applicant has submitted a new complete claim set showing marked up claims with insertions indicated by underlining and deletions indicated by strikeouts and/or double bracketing.

Please amend pending claims 1-7 as noted below.

Please add new claims 8-26 as noted below.

Listing of the Claims

1. (Currently Amended) A numeric counter oscillator comprising:

a quotient accumulator, the quotient accumulator having a programmable input for receiving a QUOTIENT value, a reference clock input and a multi-bit output, the output adapted for transmitting an output value OUT representing an accumulated quotient sum, the multi-bit output incrementing ~~by a predetermined amount~~ in response to each reference clock period;

a remainder accumulator, the remainder accumulator having programmable inputs for receiving respective REMAINDER and DIVISOR values, a reference clock input and a multi-bit output representing an accumulated digital remainder sum less than a predefined digital integer, the remainder accumulator further comprising:

a) an arithmetic circuit having an output representing accumulated remainder values; and

b) circuitry ~~a comparator~~ having a first input for receiving a programmed divisor value, and a second input for receiving the ~~remainder accumulator multi-bit output,~~ output of the arithmetic circuit, the circuitry ~~comparator~~ operative to generate an increment carry signal for application to the quotient accumulator when the remainder multi-bit output of the arithmetic circuit exceeds a ~~reaches the predefined integer~~ value dependent on the programmed divisor value.

2. (Currently Amended) A numeric counter oscillator according to claim 1 wherein the quotient accumulator comprises:

a ~~shift~~ register having a clock input for receiving the input reference clock signal;

a first summing stage for receiving the quotient value input, and comprising a second input coupled to the quotient accumulator output; and

a second summing stage disposed in series with the first summing stage and having an input coupled to the ~~comparator~~ output of said circuitry in the remainder accumulator to receive the carry increment signal, the second summing stage further comprising an output coupled to the input of the ~~shift~~ register.

3. (Currently Amended) A numeric counter oscillator according to claim 1 wherein: the circuitry of the remainder accumulator comprises[[÷]]

~~a third summing stage having an input for receiving the REMAINDER value;~~

a subtractor having an output and ~~with~~ a pair of inputs for receiving, [[m]] respectively, the ~~summed~~ output ~~from~~ of the ~~third summing stage~~ arithmetic circuit and the DIVISOR value; a multiplexer having a first switched input connected to the output of the arithmetic circuit and a second switched input connected to the output of the subtractor, and a control input connected to the output of the comparator; and

the remainder accumulation additionally comprises a second ~~shift~~ register for incrementing the remainder accumulator output in response to the input clock, wherein the remainder value and the output of the second register are provided as inputs to the arithmetic circuit ~~and feeding back the output to the third summing stage~~.

4. (Currently Amended) A numeric counter oscillator for providing a numerical solution to the relationship A/B, where B comprises a DIVISOR, and the decimal solution comprises a QUOTIENT + REMAINDER, the numerical counter oscillator comprising:

~~means for accumulating a quotient sum in response to an input QUOTIENT value; and~~

means for generating a remainder sum in response to a REMAINDER input value and a DIVISOR input value, the means for generating a remainder sum comprising means for generating a carry signal ~~to increment the quotient sum when~~ based on the relative values of the remainder sum ~~equates to~~ and the DIVISOR input value;

means for accumulating a quotient sum in response to an input QUOTIENT value and for adjusting the quotient sum in response to the carry signal.

5. (Currently Amended) A numeric counter oscillator according to claim 4 wherein the means for accumulating a quotient sum comprises:

a quotient accumulator, the quotient accumulator having a programmable input for receiving a QUOTIENT value, a reference clock input and a multi-bit output, the output adapted for transmitting an output ~~vaule~~ value OUT representing an accumulated quotient sum, the multi-bit output incrementing by a predetermined amount in response to each reference clock period.

6. (Currently Amended) A numeric counter oscillator according to claim 4 wherein the means for accumulating a remainder sum comprises:

a remainder accumulator, the remainder accumulator having programmable inputs for receiving respective REMAINDER and DIVISOR values, a reference clock input and a multi-bit output representing an accumulated digital remainder sum less than a predefined digital integer, the remainder accumulator further comprising a comparator having a first input for receiving a programmed divisor value, and a second input for receiving the remainder accumulator multi-bit output, the comparator operative to generate the ~~an increment~~ carry signal ~~for application to the quotient accumulator when the remainder multi-bit output reaches the predefined integer value~~.

7. (Currently Amended) A method of generating a desired numeric counter oscillator frequency based on a reference frequency, the desired frequency and reference frequency having the relationship A/B, where B comprises a DIVISOR, and the ~~decimal solution comprises~~ relationship may be expressed as a QUOTIENT + REMAINDER, the method including the steps:

generating a reference clock having the reference frequency and period;

incrementing a first accumulator at times related to the period of the ~~for each~~ reference clock ~~waveform period~~, the first accumulator having a QUOTIENT input and an output for keeping track of an accumulated sum;

incrementing a second accumulator at times related to the period of the reference clock, ~~counter by each reference waveform period,~~ the second accumulator ~~counter~~ having a divisor input DIVISOR, the second accumulator tracking ~~related to the QUOTIENT input for keeping track of~~ a remainder sum; and

comparing a value derived from the remainder sum to the DIVISOR input, and when said value ~~the remainder sum~~ reaches the DIVISOR value, generating a carry increment for accumulation in the first accumulator ~~counter~~.

8. (New) A method of generating a variable frequency clock using the method of claim 7 further comprising:

a) specifying values of the QUOTIENT, REMAINDER and DIVISOR to provide the desired clock frequency; and

b) using the output of the first accumulator to control a direct digital synthesis circuit.

9. (New) A method of generating a variable frequency clock using the method of claim 7 further comprising:

a) specifying values of the QUOTIENT, REMAINDER and DIVISOR to provide the desired clock frequency;

b) using the output of the first accumulator to select a value representative of a point on a periodic wave form;

c) converting the selected values to an analog signal; and

d) conditioning the analog signal to provide a clock.

10. (New) A variable frequency clock generator using the numeric counter oscillator of claim 1, additionally comprising;

a) a look-up table coupled to the output of the quotient accumulator, the look-up table providing output values representing entries in the table indexed by the output of the quotient accumulator;

b) a digital to analog converter having a digital input coupled to the output of the look-up table; and

c) a conditioning circuit coupled to the output of the analog to digital converter, the output of the conditioning circuit providing a variable frequency clock.

11. (New) The variable frequency clock generator of claim 10 wherein the look-up table stores values representing samples of a sine wave.

12. (New) The variable frequency clock generator of claim 10 wherein the conditioning circuit comprises a filter, a clipping circuit, and a phase locked loop.

13. (New) A variable frequency clock generator, comprising:

a) a numeric counter oscillator, comprising:
   i) a first control input;
   ii) a second control input;
   iii) a clock input;
   iv) a digital output having a value that changes at a plurality of times correlated to the clock input, wherein at a first subset of said times, the value of the digital output changes in proportion to the value of the first control input and, at a second subset of said plurality of times, the value of the digital output changes in proportion to the value of the first control input combined with an adjustment value, the timing of the second subset of said plurality of times depending on the value of the second control input;

b) a conversion circuit having an input and a digital output, the input coupled to the output of the numeric counter oscillator and the digital output of the conversion circuit taking on a value dictated by the input;

c) a digital to analog converter having a digital input coupled to the digital output of the conversion circuit and an analog output; and

d) a conditioning circuit having an analog input connected to the output of the digital to analog circuit and an output providing a second clock with a frequency that varies in relation to the value of the first control input and/or the second control input.

14. (New) The variable frequency clock generator of claim 13 wherein the numeric counter oscillator comprises a third control input, and the timing of the second subset of times is selected in response to the values of the second control input and the third control input.

15. (New) The variable frequency clock generator of claim 14 wherein the value of the first, second and third control inputs are selected from a desired ratio wherein the value of the first control input is the whole number quotient when the ratio is evaluated as a fraction, the value of the second control input is the whole number remainder when the quotient is computed and the value of the third control input is the divisor when the quotient is computed.

16. (New) The variable frequency clock generator of claim 14 wherein the value of the first, second and third control inputs are selected from a desired ratio wherein the value of the first control input is the whole number quotient when the ratio is evaluated as a fraction, the value of the second control input is the divisor when the quotient is computed and the value of the third control input is the whole number remainder when the quotient is computed.

17. (New) The variable frequency clock generator of claim 15 wherein the frequency of the second clock is proportional to the frequency of the clock multiplied by the ratio.

18. (New) The variable frequency clock generator of claim 13 wherein the clock input is a fixed frequency clock.

19. (New) The variable frequency clock generator of claim 13 wherein the conversion circuit is a lookup table.

20. (New) The variable frequency clock generator of claim 19 wherein the lookup table stores a series of values defining a cycle of a periodic waveform.

21. (New) The variable frequency clock generator of claim 20 wherein the periodic waveform is a sinusoid.

22. (New) The variable frequency clock generator of claim 13 wherein the digital output of the numeric counter oscillator has a maximum value N and increases to the value of the digital output are computed modulo N.

23. (New) The variable frequency clock generator of claim 13 wherein the variable frequency clock generator operates to produce a periodic signal through direct digital synthesis.

24. (New) Automatic test equipment employing the variable frequency clock generator of claim 13.

25. (New) The variable frequency clock generator of claim 14 wherein the numeric counter oscillator comprises:

a) a first accumulator, increasing by the value of the first control input at the first subset of the plurality of times, and

b) a second accumulator, increasing by the value of the second control input at the first plurality of times;

c) wherein the second subset of the plurality of times is determined by the value in the second accumulator increasing beyond the value of the third control input and at the second subset of the plurality of times,

i) the value in the second accumulator is set to the value in the second accumulator minus the value of the third control input and

ii) the value in the first accumulator is increased by the value of the first control input plus one.

26. (New) The variable frequency clock generator of claim 25 wherein,

a) the first accumulator increases values modulo N, N being a predetermined value; and

b) the second accumulator increases in value modulo B, where B is a value selected based on the value of the third control input.